WHAT IS CLAIMED IS:

1. A data transferring apparatus of liquid ejection data, comprising:

two independent buses which are a system bus and a local bus;

a main memory coupled to said system bus, capable of transferring data;

a local memory coupled to said local bus, capable of transferring data; and

a decode unit comprising a decode circuit coupled between said system bus and said local bus, capable of transferring data mutually and developing liquid ejection data compressed to be developed in line based on hardware.

2. A data transferring apparatus of liquid ejection data, comprising:

two independent buses which are a system bus and a local bus;

a local memory coupled to said local bus, capable of transferring data; and

a decode unit comprising:

a decode circuit coupled between said system bus and said local bus, capable of transferring data mutually and developing liquid ejection data compressed to be developed in line based on hardware;

a line buffer for storing liquid ejection data developed by said decode circuit per word unit; and

a DMA-transferring means for DMA-transferring liquid ejection data compressed to be developed in line from said main memory to said decode circuit, DMA-transferring liquid ejection

data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to a register of an liquid ejection head sequentially.

3. A data transferring apparatus of liquid ejection data as claimed in claim 2, wherein registers of said main memory, said decode unit and said liquid ejection head are incorporated in an ASIC as a circuit block, and registers of said decode unit and said liquid ejection head are coupled through an exclusive bus in said ASIC.

4. A data transferring apparatus of liquid ejection data as claimed in claim 2, wherein said line buffer comprising two sides of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by said decode circuit is sequentially stored in one of said sides and liquid ejection data developed by said decode circuit is sequentially stored in the other of said sides when developed data of predetermined words has been accumulated, while developed data of predetermined words is DMA-transferred to said local memory for each predetermined words when developed data of predetermined words has been accumulated.

5. A data transferring apparatus of liquid ejection data as claimed in claim 2, wherein data transfers with respect to said local bus from said decode circuit to said local memory and from said local memory to a register of said liquid ejection head are performed in a burst transfer.

6. A data transferring apparatus of liquid ejection data as claimed in claim 1, wherein said compressed liquid ejection data is run length compressed data, and said decode circuit is capable of developing run length compressed data based on hardware.

7. A data transferring apparatus of liquid ejection data as claimed in claim 2, wherein said decode unit comprises a means for storing uncompressed liquid ejection data DMA-transferred from said main memory without developing by said decode circuit based on hardware.

8. A liquid ejection apparatus comprising said data transferring apparatus of liquid ejection data as claimed in claim 1.